

Three-phase inverter current hysteresis control





Overview

How hysteresis works in a 3 phase inverter?

This technique was called current control technique by comparing the line current with the reference current. Thus, the hysteresis will force the line current to track the reference current by creating the pulse width modulation (PWM) signal. The signal was fed into the gate driver circuit and injecting the output to the three phase inverter.

What is a hysteresis current controller (three-phase) block?

The Hysteresis Current Controller (Three-Phase) block implements three-phase hysteresis current control for power converters. Control the currents in a BLDC based electrical drive using hysteresis controllers. A DC voltage source feeds the BLDC through a controlled three-phase inverter.

What are hysteresis current controller techniques for grid connected inverters?

The purpose of this paper is to present a comparative study on basic hysteresis current controller techniques for grid connected inverters. Hysteresis current controllers are best known for robustness, fast error tracking, better dynamic response and ease of implementation than other controllers proposed in literature.

What is hysteresis current control technique?

This project was an overview of the development on Hysteresis Current Control Technique which could be applied to the three phase induction motor. The objective of the controller was to control the current that supply into the induction motor.



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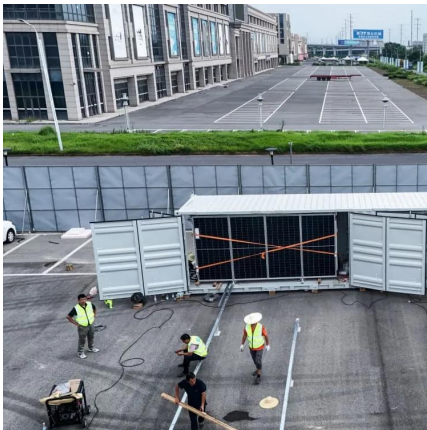
A hysteresis loop control method for output current of three-phase

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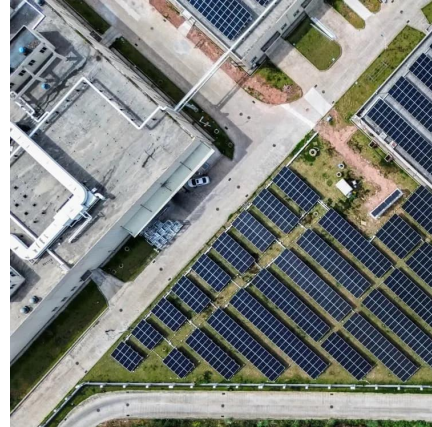
Software Resources
Implementation of The Hysteresis Current Control
FPGA Logic of The Hysteresis Controller
CPU Implementation
Experimental Results and Validation of The Hysteresis Current Control
This implementation stems from the following choices: 1. The current references are generated inside the CPU at a 40 kHz interval. 2. The measured 3-phase currents are sampled at 400 kHz. 3. The hysteresis control is implemented inside the programmable logic area (FPGA) by comparing the "fast" measured currents (400 kHz) with the "slow" generated r See more on imperix Springer

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